The opinion in support of the decision being entered today was ***not*** written for publication and is ***not*** binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte LEONARD FORBES and KIE Y. AHN

Appeal No. 2005-1205
Application 08/903,453

ON BRIEF

Before WARREN, OWENS and WALTZ, *Administrative Patent Judges*.

WARREN, *Administrative Patent Judge*.

Decision on Appeal

This is an appeal under 35 U.S.C. § 134 from the decision of the examiner finally rejecting claims 2, 3, 24 through 28, 41 through 48, 50 through 52 and 65 through 68, all of the claims in the application.

Claims 3, 46 and 68 illustrate appellants' invention of a transistor having an amorphous carburized silicon insulative layer grown on the substrate between the channel region and a floating gate, that can be used in a memory device, and are representative of the claims on appeal:

3. An integrated circuit memory device supported by a semiconductor substrate, the device comprising:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate supported by the substrate and extending between the source and the drain above the channel;

a control gate formed adjacent to and insulated from the floating gate; and

an insulative layer of amorphous carburized silicon grown on the channel and located between the channel and the floating gate.

46. A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate; and

a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

68. A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate;

a floating gate; and

means for separating the floating gate from the channel region.

The references relied on by the examiner are:

Sugita et al. (Sugita)[1] (Japanese Kokai Patent Publication)	08-255878	Oct. 1, 1996

Stanley G. Burns et al. (Burns), "Semiconductor Memories," *Principles of Electronic Circuits* 382-83 (St. Paul, West Publishing Company. 1987).

I. Sakata et al. (Sakata), "Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures," 30 *Electronic Letters* no. 9, 688-89 (April 1994).

Appellants have relied on the following references:

Q.-D. Qian et al. (Qian), "Multi-day Dynamic Storage of Holes at the AlAs/GaAs Interface," EDL-7 *IEEE Electron Device Letters* no. 11, 607-09 (November 1986).

Federico Capasso et al. (Capasso), "New Floating-Gate AlGaAs/GaAs Memory Devices with Graded-Gap Electron Injector and Long Retention Times," 9 *IEEE Electron Device Letters* no. 8, 607-09 (August 1988).

J.A. Lott et al. (Lott), "Anisotropic thermionic emission of electrons contained in GaAs/AlAs floating gate device structures," 55 *Appl. Phys. Lett.* no. 12, 1226-28 (September 1989).

---

[1] We refer in our decision to the translation of Sugita submitted by appellants with the IDS filed August 30, 1999.

The examiner has rejected appealed claims 2, 3, 24 through 28, 41 through 48, 50 through 52 and 65 through 68 under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita and Burns (answer, pages 3-6).[2]

Appellants group the appealed claims but separately argue only claims 46 and 68 (brief, pages 3, 5 and 18). Thus, we decide this appeal based on these appealed claims. 37 CFR § 1.192(c)(7) (2003); *see also* 37 CFR § 41.37(c)(1)(vii) (September 2004).

We affirm.

Rather than reiterate the respective positions advanced by the examiner and appellants, we refer to the answer and to the brief and reply brief for a complete exposition thereof.

Opinion

We have carefully reviewed the record on this appeal and based thereon find ourselves in agreement with the supported position advanced by the examiner that, *prima facie*, the claimed transistor encompassed by appealed claims 46 and 68 would have been obvious over the combined teachings of Sakata, Sugita and Burns to one of ordinary skill in this art at the time the claimed invention was made. In view of the established *prima facie* case of obviousness, we again consider the record as a whole with respect to this ground of rejection in light of appellants' rebuttal arguments in the brief and reply brief. *See generally, In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

Our consideration of the application of the cited prior art to claim 46 requires that we first interpret the claim language thereof by giving the claim terms their broadest reasonable interpretation in light of the written description in the specification as interpreted by one of ordinary skill in the art, without reading into the claim any limitation or particular embodiment disclosed in the specification. *See, e.g.*, *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); *In re Donaldson Co., Inc.*, 16 F.3d 1189, 1192-95, 29 USPQ2d

---

[2] The examiner states that grounds of rejection of the appealed claims over "Lott et al. in view of Sakata or Lott et al. in view of Sakata and Burns, are hereby withdrawn" (answer, page 6). These grounds of rejection are set forth at pages 7-10 of the final rejection mailed July 15, 2003, and do not involve Lott relied on in the ground of rejection under § 103(a) advanced on appeal.

1845, 1848-50 (Fed. Cir. 1994) (*en banc*); *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The plain language of claim 46 encompasses any form of a transistor that comprises at least a substrate having source and drain regions separated by a channel region, and a layer of amorphous carburized silicon, that is, amorphous silicon carbide (a-SiC), grown on the substrate and separating the channel region and a floating gate. The transitional term "comprising" opens claim 46 to include transistors having such additional elements and materials as an additional layer or layers including a control gate formed adjacent to and insulated from the floating gate, as well as electrodes on the source and drain regions and the control gate, and indeed, any other elements of any manner of integrated memory device such as encompassed by appealed claim 3. *See*, e.g., *Vehicular Technologies Corp. v. Titan Wheel Int'l Inc.*, 212 F.3d 1377, 1383, 54 USPQ2d 1841, 1845 (Fed. Cir. 2000); *Exxon Chem. Pats., Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1555, 35 USPQ2d 1801, 1802 (Fed. Cir. 1995) ("The claimed composition is defined as comprising - meaning containing at least - five specific ingredients."); *In re Baxter*, 656 F.2d 679, 686-87, 210 USPQ 795, 802-03 (CCPA 1981) ("As long as one of the monomers in the reaction is propylene, any other monomer may be present, because the term 'comprises' permits the *inclusion* of other steps, elements, or materials.").

We find that Sakata would have disclosed to one of ordinary skill in this art that experiments with an aluminum (Al) ohmic contact/n- or p-type crystalline Si (c-Si)/graded hydrogenated amorphous silicon carbide (a-SiC:H)/ hydrogenated amorphous silicon (a-Si:H)/ a-SiC:H/Al metal gate diode (Sakata **Fig. 1** and "*Sample Preparation*," page 688) resulting in the "*Capacitance-voltage characteristics*" of a sample diode having an n-type substrate shown in Sakata **Fig. 2**, "confirm that the [a-SiC:H/a-Si:H heterojunctions] structure shown in **Fig. 1** can be applied to floating-gate memory devices" which operate as follows:

> With the application of positive (negative) bias to the metal gate, electrons (holes) are efficiently injected from the crystalline Si (c-Si) substrate into the thin a-Si:H layer through the compositionally graded a-SiC:H layer. When the bias voltage is restored to zero, injected electrons(holes) can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces. By applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons and thus the memory is erased. [Page 688, cols. 1-2.]

Sakata reports the basis for this in "*Results and discussion*," suggesting that the graded a-SiC:H/a-Si:H "structure can be used as a component of dynamic random access memories (DRAMs) at room temperature [footnote omitted.]" (pages 688-89). Sakata states in "*Conclusion*" that "band-engineered a-Si:H/a-SiC:H heterojunctions on c-Si can be applied to electrically programmable and erasable memory devices because both electrons and holes can be conducted through undoped a-SiC:H and can be stored in a-Si:H" as "[i]t has been confirmed that the graded a-SiC:H and the a-Si:H act as the carrier injection layer and the memory trap site, respectively" (page 689).

We find that Sugita would have disclosed to one of ordinary skill in this art floating gate transistors such as that illustrated in Sugita **Fig. 1** in which polycrystalline silicon carbide (β-SiC) insulating layer **5** can be grown on a p-type silicon substrate **1** over the channel region between source region **2** and drain region **3**, after which SiO_2 layer **4** is formed at the interface between silicon substrate **1** and β-SiC layer **5**, thus separating the channel region from polysilicon floating gate **6** which is isolated from control grate **8** by SiO_2 layer **7**, and with source electrode **9**, drain electrode **10** and an electrode on control gate **8** as shown; and would have acknowledged in **Fig. 3**, a "conventional floating gate transistor" which differs from that of Sugita **Fig. 1** in the absence of SiO_2 layer **4** (pages 2-3, 7-8, 10-11 and 16-19).

We find that the conventional floating gate transistor acknowledged by Sugita and floating gate transistors disclosed in this reference differ from the claimed transistor encompassed by claim 46 in the presence of β-SiC rather than a-SiC. However, Sugita would have disclosed to this person that the silicon carbide (SiC) layer can be any form of SiC (e.g., page 7, [0017]), and particularly that "in the above–mentioned application example [at pages 10-11, referring to **Fig. 1**], polycrystalline β-SiC is used as the SiC component of the gate insulating film" but "a polycrystalline crystal need not be used: *amorphous* . . . may also be adopted" (page 13, [0041]; italics emphasis added).[3]

[3] It is well settled that a reference stands for all of the specific teachings thereof as well as the inferences one of ordinary skill in this art would have reasonably been expected to draw therefrom, *see In re Fritch*, 972 F.2d 1260, 1264-65, 23 USPQ2d 1780, 1782-83 (Fed. Cir. 1992); *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968), presuming skill on the part of this person. *In re Sovish*, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985).

We find that the acknowledged conventional floating gate transistor and the disclosed floating gate transistors are taught by Sugita to operate as a component of DRAM integrated circuit memory devices, wherein the electron barrier between the silicon substrate and an SiC film grown on the substrate is adjusted with an SiO_2 layer to permit tunnel conduction and provide an appropriate refresh time (e.g., pages 4-6, 8-9 and 11-12). In this respect, the SiO_2 layer of the disclosed floating gate transistor which can be formed in the silicon substrate after the SiC film is formed on that substrate, is no more than 3 nm thick and has no insulative properties (e.g., page 8, [0019] and [0020], page 9, [0025], and page 11, [0033]).

We find that Burns would have similarly disclosed to one of ordinary skill in this art that erasable programmable read-only memories (EPROMs) comprising an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) having a source region and a drain region in a p-type substrate, an insulative gate oxide layer, a floating gate, an insulating layer and a select gate as shown in Burns **Fig. 9.10(b)** (page 382). We find that the "select gate" of Burns is functionally equivalent to the "control gate" of Sugita. Burns would have taught that when "a high voltage . . . is applied to the drain and to the select gate . . . [a] channel is established" such that "[e]lectrons are accelerated in the high field between source and drain, and acquire enough energy to enter the conduction band of the gate oxide layer" where "they are attracted by the positive potential on the select gate, and many of them lodge on the floating gate," thus trapping electrons on the floating gate when the voltage is removed (pages 382-83). Burns further teaches that illuminating the device with ultraviolet light, the trapped electrons obtain sufficient photon energy to escape the floating gate through the oxide layer (page 383).

The examiner finds that the a-SiC:H layer containing device having an Al contact on each end disclosed by Sakata for application to floating gate memory devices, differs from the claimed floating gate transistor encompassed by claim 46 in the absence of source, drain and channel regions in the n- or p- type c-Si substrate of that device (answer, pages 3-4). The examiner determines that one of ordinary skill in the art would have formed such regions in the c-Si substrate of Sakata as suggested by the use of the same regions in the p-type silicon substrates of the floating gate transistors taught by Sugita and Burns in the expectation of successfully modifying the device of Sakata to form a floating gate transistor useful as a component in

integrated circuit memory devices in the same or similar manner as the floating gate transistors of Sugita and Burns (answer, pages 3-5).

Appellants submit that "there is no suggestion or motivation to form a device by combining elements from" Sakata, Sugita and Burns. In this respect, appellants first contend that "[t]here are substantial difference between the principles of operation of the floating gate transistor of Sakata" which conducts "both electrons and holes" and "the principles of operation of the floating gate transistor of Sugita" (brief, pages 7-8). While appellants contend that "[t]he known principles of operation of a floating gate transistor such as Sugita are substantially different," they then discuss the teachings of Burns, arguing that "[u]nlike the operation of the HJ diode structure of Sakata, only electrons are involved in programming and erasing a floating gate transistor according to Burns" (brief, page 8). Appellants further argue that adding the regions proposed by the examiner to the device of Sakata would change "the basic principles under which the Sakata construction was designed to operate," and that there is no evidence that such principles would not be changed (*id.*). Appellants then contend that Sakata suggests that the structure shown therein can be used in a DRAM device, relying on Qian (brief, pages 8-9). In view of the clear suggestion that we find in Sakata in this respect (*see above* p. 5), it is not necessary that we discuss Qian.

Appellants next submit in this respect that Sakata's statement suggesting that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices" is not a clear teaching that would have motivated one of ordinary skill in the art to modify Sakata's device as proposed by the examiner, and contends that Sakata "teaches away from" the combination of Sakata, Sugita and Burns (brief, page 9). Appellants point to Sakata's reference to Capasso as reporting "similar memory devices based on AlGaAs/GaAs HJ," and allege that thus "Sakata is referring to the earlier statement in the same paragraph . . . that 'the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices'" (brief, pages 9-10). Appellants state that "Capasso reports AlGaAs/GaAs floating-gate memory devices" but "does not show a picture of the device," quoting the following part of Capasso's abstract with respect to the operation of such devices:

> Compared with conventional Si-based floating-gate devices this structure operates on a different injection method. Electrons are injected from the control gate into the

floating gate using an AlGaAs graded-gap barrier. [Capasso, page 377, col. 1; brief, page 10.]

Appellants contend that Sakata thus would have indicated to one of ordinary skill in the art "that a floating gate device with its heterojunction operates like Capasso's memory device that injects electrons from the control gate into the floating gate" (brief, page 10). Appellants argue that this is a different principle of operation than taught by Burns as well as by Sugita who "describes tunnel conduction at the interface between the silicon substrate 1 and the SiC film 5 in paragraphs [0019] and [0020]" and "electrons stored in the cell 22 escape to the source and drain side by Fowler-Nordheim type tunnel injection in paragraph [0040]," wherein "source 2 and drain 3 are shown in the silicon substrate 1 of Sugita" (brief, page 10).

Appellants further rely on [Lott] in this respect, stating that "[Lott] refers to the [GaAs/AlAs floating gate device therein] as '[o]ur vehicle (Fig. 1) has a vertical structural similar to that of [Capasso]'" (brief, pages 10-11). Appellants describe the GaAs/AlAs floating gate device of [Lott] as "[t]he floating . . . is between the source and drain on one side and the channel on the other side [of a superlattice], and separates the source and the drain from the channel" (brief, pages 11-12). Appellants allege that "[t]he transistor structure shown in Figure 1 of [Lott] is linked by Sakata and [Lott] through Capasso to Sakata's earlier statement that 'the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices" (brief, pages 11-12). On this basis, appellants advance the position that the alleged connection between the floating gate devices of the references is evidence to one of ordinary skill in the art "to use the heterojunction of Sakata in a transistor such [*sic*, as] that in [Lott]," and thus that "[t]he structures of [Lott] and Sugita and Burns are substantially different, and there is no comparable suggestion in the prior art to form a device combining elements from Sakata, Sugita and Burns" (brief, page 12).

The examiner responds that the addition of source, drain and channel regions to the substrate of the Sakata as proposed based on the combined teachings of Sakata, Sugita and Burns "would *not* alter the manner in which electrons are stored on or erased from the floating gate" of the device of Sakata because the reference establishes that "the device is programmed and erased by application of specific voltage to the control gate" (answer, pages 14-15; italics emphasis in

original).[4] The examiner further points out that the structure of the device of Sakata "is nothing more than a simple capacitor; two plates with a dielectric therebetween" and "[t]he C-V plot of Sakata's figure 2 is simply showing the capacitance between the floating gate and the substrate" as explained under *Results and Discussion* in that reference (answer, page 16). With respect to Capasso, the examiner finds that the principle of operation set forth in the abstract of this document as cited by appellants, "directly contradicts the clear teachings of Sakata, as quoted by appellant [*sic*]; 'electrons . . . are efficiently injected *from the crystalline Si (c-Si) substrate*," and thus that "[a]s such, Sakata does *not* operate like Capasso" (answer, page 17, italics emphasis in original). With respect to Lott, the examiner points out that "[Lott], like Capasso, forms its device in an AlGaAs based substrate" and "there is no suggestion, *anywhere* that the silicon-based device would, or even could, form a source and drain next to the floating gate as shown in [Lott's] AlGaAs device," while Sugita and Burns teach the formation of source and drain regions in a substrate like Sakata's (answer, page 18; italics emphasis in original).

Appellants reply that Sakata's statement that the HJ structure therein is applicable to floating gate memory devices is not established by Sugita and Burns because the examiner has provided "no evidence that all floating gate devices formed in silicon are similar to that of Sugita or Burns," and Lott "is evidence that devices categorized as floating gate devices do not necessarily have the structure of Sugita" (reply brief, pages 2-3). Appellants further contend that there is no evidence that the device of Sakata having a source and drain of the device of Sugita "would be able to inject holes from the Si substrate into 'the thin a-Si:H layer through the compositionally graded a-SiC:H layer," and thus, "the addition of the source and drain would require a change in the basic principles under which the Sakata construction was designed to operate" (reply brief, pages 3-4).

---

[4] We have not considered any of the additional references that examiner relies on to support the ground of rejection in response to appellants' arguments (answer, e.g., pages 9, 11, 13-14, 18 and 19) because these references are not included in the statement of the ground of rejection (answer, page 3). Reliance on a reference to support a ground of rejection that is not included in the statement of the rejection is clearly impermissible. *See In re Hoch*, 428 F.2d 1341, 1342 n. 3, 166 USPQ 406, 407 n.3 (CCPA 1970); *cf. Ex parte Raske*, 28 USPQ2d 1304, 1304-05 (Bd. Pat. App. & Int. 1993).

Our consideration of the record as a whole in light of appellants' arguments leads us to agree with the examiner. Appellants disclose in the written description in their specification that the principal element of the claimed floating gate transistor encompassed by claim 46 that is different from floating gate transistors of the prior art used in integrated circuit memory devices is the layer of a-SiC grown on the c-Si substrate and separating the channel region and the floating gate (e.g., pages 1-3, particularly, page 3, ll. 5-9). In this respect, we find that the closest applied prior art is Sugita which would have taught forming an a-SiC layer over the channel region of a silicon substrate, separating the channel region and the floating gate, in preparing a floating gate transistor component for a DRAM integrated circuit memory device (*see above* p. 6). The a-SiC layer containing floating gate transistors of Sugita have an electrode on the source and drain regions of the substrate and on the control gate. Thus, the a-SiC layer containing floating gate transistors of Sugita satisfy all of the elements of claim 46.

In similar manner to the a-SiC layer containing floating gate transistors of Sugita, the device of Sakata **Fig. 1** has an a-SiC:H layer formed on a c-Si substrate that has an ohmic contact on its backside, and an electrode on the metal gate, which device is suggested by the reference to be used as a component in DRAM integrated circuit memory devices (*see above* pp. 4-5). Both references similarly describe the operation of the devices disclosed therein as the application of voltage to the substrate and the control or metal gate causes electrons in the substrate to enter the a-SiC or a-SiC:H insulative layer and lodge in the polysilicon or a-Si:H floating gate.

Thus, we are of the view that as the examiner submits, the combined teachings of Sakata and Sugita would have reasonably suggested to one of ordinary skill in this art that the c-Si substrate of the floating gate device of Sakata can be modified to have the electrode on the substrate in a source region which is paired with drain and channel regions as in the structurally related floating gate electrode of Sugita, in the reasonable expectation of forming a floating gate transistor having an a-SiC:H layer formed between the c-Si substrate and the floating gate, which can be used as a component of a DRAM integrated circuit memory device. We are reinforced in our view by Burns which would have taught a floating gate transistor with the same or similar silicon substrates having source, drain and channel regions which operates in the same manner when a voltage is applied to the source region and the select, that is, control, gate, and can be

used as a component of integrated circuit memory devices. *See In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981)("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.").

We are not persuaded otherwise by appellants' arguments based on Capasso and Lott. We find no evidence in this record establishing that the device of Sakata "injects electrons from the control gate into the floating gate" as appellants contend based on a mere reference to Capasso by Sakata. We agree with the examiner's finding that the statement of operation in the abstract of Capasso of a metal layer transistor structure, that appellants cannot otherwise identify except that it has control gate and floating gate functional structures, is directly contrary to the principle of operation stated by Sakata at page 688, col. 1, based on results discussed in Sakata for the disclosed silicon based floating gate structure. Indeed, the clear statement in Capasso's abstract that "[c]ompared with conventional Si-based floating-gate devices this structure operates on a different injection method" cannot be discounted in the absence in the record of a scientific explanation or additional evidence that address this point. Like the examiner, we find no such explanation or evidence in Lott as relied on by appellants. Indeed, the metal layer floating gate structure of Lott appears to be similar to the metal layer floating gate structure of Capasso, and as appellants admit, the functional elements of the device of Lott are arranged differently than the functional elements of the silicon-based floating gate structure of Sakata. Thus, there is little, if any, evidence in the record supporting appellants allegation that the metal layer floating gate device disclosed in Lott is linked through the metal layer floating gate device of Capasso to the silicon based floating gate device of Sakata.

We are also unpersuaded by appellants' arguments that the principle of operation of the silicon based floating gate device of Sakata described with respect to "electrons and holes" therein, differs from the principle of operation of the silicon based transistors of Sugita and Burns which are described in each reference with respect to "electrons." We found above that the principles of operation is similarly described in each of these references with respect to the

application of voltage causing electrons in the silicon substrate to enter the silicon based insulative layer and lodge in the silicon based floating gate. The fact that Sakata additionally describes the operation of the device therein in terms of electron holes while Sugita and Burns do not, does not alone establish a difference in the principles of operation of floating gate devices that are structurally related. Thus, the burden rests with appellants to submit scientific argument and/or objective evidence to establish their position. *See, e.g., In re Best*, 562 F.2d 1252, 1255-56, 195 USPQ 430, 433-34 (CCPA 1977)("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product. See *In re Ludtke*, [441 F.2d 660, 169 USPQ 563 (CCPA 1971)]. Whether the rejection is based on "inherency" under 35 USC § 102, on "prima facie obviousness" under 35 USC § 103, jointly or alternatively, the burden of proof is the same, and its fairness is evidenced by the PTO's inability to manufacture products or to obtain and compare prior art products. [Footnote and citation omitted.]"). In the absence of such scientific argument or evidence, appellants' mere arguments in this respect are entitled to little, if any, weight. *See In re De Blauwe*, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984); *In re Payne*, 606 F.2d 303, 315, 203 USPQ 245, 256 (CCPA 1979); *In re Lindner*, 457 F.2d 506, 508, 173 USPQ 356, 358 (CCPA 1972).

Thus, on this record, the combined teachings of Sakata, Sugita and Burns provide substantial evidence in support of the examiner's position. Accordingly, we are of the opinion that one of ordinary skill in this art routinely following the combined teachings of these references would have reasonably arrived at the claimed floating gate transistor encompassed by appealed claim 46, including each and every limitation thereof arranged as required therein, without resort to the written description in appellants' specification. *See In re Dow Chem. Co.*, 837 F.2d 469, 473, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988) ("The consistent criterion for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that [the claimed process] should be carried out and would have a reasonable likelihood of success viewed in light of the prior art. [Citations omitted] Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure.").

Furthermore, we found above that Sugita would have taught one of ordinary skill in this art that a-SiC can be used as an insulating layer in place of the β-SiC layer in the floating gate transistors of Sugita as illustrate in **Fig. 1** and as acknowledged by this reference as illustrated in **Fig. 3**, thus arriving at a-SiC containing floating gate transistors with a reasonable expectation of successfully using the same in integrated circuit memory devices. Therefore, one of ordinary skill in this art routinely following the teachings of Sugita alone would have reasonable arrived at claimed transistors encompassed by claim 46, including each and every limitation arranged as required by the claim, without resort to the written description in appellants' specification and claims. *See B.F. Goodrich Co. v. Aircraft Braking Sys. Corp.*, 72 F.3d 1577, 1582, 37 USPQ2d 1314, 1318 (Fed. Cir. 1996) ("When obviousness is based on a particular prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. [Citation omitted.] This suggestion or motivation need not be expressly stated. [Citation omitted.]"); *Merck & Co., Inc. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807, 10 USPQ2d 1843, 1845-46 (Fed. Cir. 1989) ("That the '813 patent discloses a multitude of effective combinations does not render any particular formulation less obvious. This is especially true because the claimed composition is used for the identical purpose. [Citations omitted.]").

Turning now to appealed claim 68, as appellants point out, this claim stands rejected under the combined teachings of Sakata, Sugita and Burns on the same basis as appealed claim 46, but the examiner has not considered the limitation "means for separating the floating gate from the channel region" in applying the applied references to this claim (brief, page 18). Thus, the "means for" claim language must be interpreted in order to review the application of prior art to the claimed invention encompassed by claim 68 because all of the claim limitations must be considered. *See, e.g., In re Geerdes*, 491 F.2d 1260, 1262-63, 180 USPQ 789, 791-92 (CCPA 1974) (In considering grounds of rejection under 35 U.S.C. § 103, "*every* limitation in the claim must be given effect rather than considering one in isolation from the others."); *cf. Donaldson*, 16 F.3d at 1195-97, 29 USPQ2d at 1850-52.

We find that the "means for separating the floating gate from the channel region" clause in claim 68 specifies "means for" the specified function but does not define structure which satisfies that function and thus, the strictures of 35 U. S. C. § 112, sixth paragraph, apply. *See*

Texas Digital Systems, Inc. v. Telegenx, Inc., 308 F.3d 1193, 1208, 64 USPQ2d 1812, 1822-23 (Fed. Cir 2002), and cases cited therein. Therefore, the "means" language in this clause must be construed as limited to the "corresponding structure" disclosed in the written description in the specification and "equivalents" thereof. *Donaldson*, 16 F.3d at 1192-95, 29 USPQ2d at 1848-50. The "corresponding structure" is that "structure in the written description necessary to perform that function [citation omitted]," that is, "'the specification . . . clearly links or associates that structure to the function recited in the claims.' [Citation omitted.]" *Texas Digital Systems*, *supra*. "[A] section 112, paragraph 6 'equivalent[]' . . . [must] (1) perform the identical function and (2) be otherwise insubstantially different with respect to structure. [Citations omitted.]" *Kemco Sales, Inc. v. Control Papers Co.*, 208 F.3d 1352, 1364, 54 USPQ2d 1308, 1315-16 (Fed. Cir. 2000). "[T]wo structures may be 'equivalent' for purposes of section 112, paragraph 6 if they perform the identical function in substantially the same way, with substantially the same result. [Citations omitted.]" *Kemco Sales,* 208 F.3d at 1364, 54 USPQ2d 1315. "[T]he 'broadest reasonable interpretation' that an examiner may give means-plus-function language is that statutorily mandated in [35 U.S.C. § 112,] paragraph six," and in this respect, the examiner should not confuse "impermissibly imputing limitations from the specification into a claim with properly referring to the specification to determine the meaning of a particular word or phrase in a claim. [Citations omitted.]" *Donaldson*, 16 F.3d at 1195, 29 USPQ2d at 1850; *see also Morris*, 127 F.3d 1048, 105556, 44 USPQ2d 1023, 1028 (explaining *Donaldson*).

Appellants neither submit an interpretation of the subject claim language nor separately argue the separate patentability of claim 68 over the applied prior art separate from claim 46 based on this language (*id.*; pages 5-13 and 18; reply brief in entirety). Appellants summarize the invention with reference to specification **FIG. 1**, stating that "a gate 106 separated from the channel region 110 by a layer of amorphous carburized silicon 118 that was grown on the substrate 108" (brief, pages 1-2).

However, the specification discloses that *any* SiC insulative film is a "means for" performing the function of "separating the floating gate from the channel region" that is "in the substrate," and provides a gate insulator for a transistor that has "a low tunneling barrier," and

thus, is not limited to "preferably" an a-SiC film (e.g., page 2, l. 18, to page 3, l. 23; col. 5, ll. 1-8 and 18-19; page 5, l. 20, to page 7, l. 13; page 7, ll. 21-23; and **FIGs. 1-3**).

Thus, claim 68 so interpreted encompasses additional and different SiC insulative films than a-SiC films for separating the channel region in the substrate from the floating gate, including α-SiC and β-SiC as disclosed in Sugita (e.g., page 13, [0041]). Therefore, the combined teachings of Sakata, Sugita and Burns apply to appealed claim 68 in the same manner that the teachings apply to appealed claim 46 as we found above because the remaining limitations in both claims are otherwise the same. In addition, the acknowledged "conventional" transistor containing β-SiC separating the channel region in the substrate from the floating gate described in Sugita **Fig. 3** anticipates appealed claim 68, which is the "ultimate of obviousness," *see In re Baxter Travenol Labs.*, 952 F.2d 388, 392, 21 USPQ2d 1281, 1284-85 (Fed Cir. 1991) (citing *In re Fracalossi*, 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982).

Accordingly, based on our consideration of the totality of the record before us, we have weighed the evidence of obviousness found in the combined teachings of Sakata, Sugita and Burns with appellants' countervailing evidence of and argument for nonobviousness and conclude that the claimed invention encompassed by appealed claims 2, 3, 24 through 28, 41 through 48, 50 through 52 and 65 through 68 would have been obvious as a matter of law under 35 U.S.C. § 103(a).

The examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv) (2004).

AFFIRMED

CHARLES F. WARREN	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
TERRY J. OWENS	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
	)	
THOMAS A. WALTZ	)	
Administrative Patent Judge	)	

Schwegman Lundberg Woessner & Kluth
PO Box 2938
Minneapolis, MN 55402